a plurality of device formation regions in which predetermined devices are to be formed respectively, said plurality of device formation regions being provided in said SOI layer;

at least one isolation region provided in said SOI layer for insulatively isolating said plurality of device formation regions from each other; and

a body region provided in said SOI layer and capable of externally fixing electric potential,

wherein at least part of said at least one isolation region includes a partial isolation region having a partial insulation region formed in an upper part thereof and a semiconductor region formed in a lower part thereof between at least two of said device formation regions, said semiconductor region serving as part of said SOI layer and being formed in contact with at least one of said plurality of device formation regions and said body region,

said semiconductor region doped with impurities of the same conductivity type as said at least one of said plurality of device formation regions and said body region.

6. (Amended) A semiconductor device having an SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer, said semiconductor device comprising:

a plurality of device formation regions in which predetermined devices are to be formed respectively, said plurality of device formation regions being provided in said SOI layer;

at least one isolation region provided in said SOI layer for insulatively isolating said plurality of device formation regions from each other; and

a body region formed in the SOI layer and capable of fixing electric potential upon application of an externally applied potential to said body region,

wherein said body region is formed in contact with one of top and bottom surfaces of at least one of said plurality of device formation regions.

23. (Amended) A semiconductor device having an SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer, said semiconductor device comprising:

a device formation region in which a predetermined device is to be formed, said device formation region being provided in said SOI layer; and

a peripheral insolation region provided in said SOI layer and surrounding said device formation region, said peripheral isolation region including a partial isolation region having a partial insulation region formed in an upper part thereof and a semiconductor region formed in a lower part thereof between at least two of said device formation regions and serving as part of said SOI layer,

wherein said semiconductor region is formed in contact with said device formation region and is floating,

said semiconductor region doped with impurities of the same conductivity type as said at least one of said plurality of device formation regions and said body region.

REMARKS

Favorable reconsideration of the present application in view of the amendment and in light of the following discussion is respectfully requested.

Initially, Applicants wish to thank the Examiner for the personal Interview with Applicants' Representatives on September 4, 2001, at which agreement was reached that the claims substantially as amended are allowable over the Saito reference (U.S. 6,100,570).